VP070 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Barinder Singh Rai, et al.	Group Art Unit:	Not Yet Assigned
Serial No.:	Unknown	Examiner:	Not Yet Assigned
Filed:	Herewith		
Title:	Low Overhead Read Buffer		

CERTIFICATION UNDER 37 CFR 1.10

"Express Mail" Mailing Label Number: EV311301526US

I hereby certify that this Information Disclosure Statement, and the documents referred to as enclosed therein are being deposited with the United States Postal Service in an envelope as "Express Mail Post Office to Addressee" under 37 CFR 1.10 on the date indicated below and is addressed to Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

Dated: July 10, 2003

Virginia Silva

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 C.F.R. §1.56, and in accordance with the practice under 37 C.F.R. §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed Form PTO-1449. Copies of the listed information are also enclosed.

This Information Disclosure Statement is being filed within three months of the U.S. filing date or before the mailing date of a first Office Action on the merits. No statement or fee is required (37 CFR §1.97(b)).

CONCLUSION

The Commissioner is hereby authorized to charge any additional fees, which may be required, or credit any over-payment to Deposit Account No.: 19-2746.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be initialed and returned indicating that such information has been considered.

Respectfully submitted,

Michael T. Gabrik
Registration No. 32,896

Please address all correspondence to:

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Intellectual Property Department
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Date: July 10, 2003

PATENT AND TRADEMARK OFFICE

Unknown	VP070
APPLICANT(S) Barinder Singh Rai, et al.	
FILING DATE Herewith	GROUP Not Yet Assigned

INFORMATION DISCLOSURE CITATION
(USE SEVERAL SHEETS IF NECESSARY)
PAGE 1 OF 1

U.S. PATENT DOCUMENTS

E.I.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	AA	2002/0135817	9/26/02	Wang			
	AB	6,401,186	6/4/02	Blodgett			
	AC	6,370,611	4/9/02	Callison, et al.			
	AD	6,219,745	4/17/01	Strongin, et al.			
	AE	6,075,740	6/13/00	Leung			
	AF	5,883,855	3/16/99	Fujita			
	AG	5,761,706	6/2/98	Kessler, et al.			
	AH	5,659,713	8/19/97	Goodwin, et al.			
	AI	5,499,355	3/12/96	Krishnamohan, et al.			
	AJ	5,461,718	10/24/95	Tatosian, et al.			
	AK	5,146,582	9/8/92	Begun			

FOREIGN PATENT DOCUMENTS

E.I.		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
	AL	11-65920	3/9/99	Japan			Abstract
	AM						
	AN						
	AO						
	AP						
	AQ						

OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	AR	**Toshio Sunaga, et al., "An Eight-Bit Prefetch Circuit for High-Bandwidth DRAMS's", *IEEE Journal of Solid-State Circuits,* Vol. 32, No. 1, January 1997, pp. 105-110.**
	AS	**Toshio Sunaga, et al., "A Full Bit Prefetch Architecture for Synchronous DRAM's", *IEEE Journal of Solid-State Circuits,* Vol. 30, No. 9, September 1995, pp. 998-1005**
	AT	**Thomas Gleerup, et al., "Memory Architecture for Efficient Utilization of SDRAM: A Case Study of the Computation/Memory Access Trade-Off", *Proceedings of the Eighth International Workshop on Hardware/Software Codesign,* 2000, pp. 51-55**

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.